What is Claimed is:

1. In a processing system having an unprotected pipeline, an apparatus comprising:

a first logic gate for providing a first signal when a control signal is applied thereto; and

a second logic gate for providing a halt signal when said first signal is applied to a first input terminal of the second logic gate and a halt request signal is applied to a second input terminal of the second logic gate.

2. The apparatus as recited in claim 1 further comprising a storage unit, wherein the storage unit stores the control signal.

3. The apparatus as recited in claim 2 wherein an interruptible code portion signal applied to a second terminal of the first logic gate, the interruptible code portion signal applied to the second terminal resulting in the generation of the first signal.

4. The apparatus as recited in claim 3 wherein the halt signal is generated by the second logic gate when the processor is executing a non-interruptible code portion and the control signal is stored in the storage unit.

5. The apparatus as recited in claim 4 wherein the first logic gate is a logic OR gate and the second logic gate is a logic AND gate.

6. A method for providing a halt request signal during the execution of a non-interruptible code portion in a processor having a non-protected pipeline; the method comprising:

when an interruptible code portion is executing, generating a halt signal in response to halt request signal; and

when a control signal is present, generating a halt signal in response to a halt request signal.

7. The method as recited in claim 6 wherein, when the control signal is present, generating a halt signal when the code is executing in an interruptible mode and when the code is executing in a non-interruptible mode.

8. The method as recited in claim 7 wherein the control signal is stored in a storage unit by a user.

9. A data processing unit comprising:

a processor, the processor including:

a non-protected pipeline,

the processor executing interruptible code and non-interruptible code;

a storage unit for storing a control bit;

a logic unit responsive to the control bit for generating a halt signal in response to a halt request signal and the control bit, the logic unit generating a halt signal is response to a halt request signal during execution of an interruptible code portion when the control bit is not stored in the storage unit.

10. The processing unit as recited in claim 9 wherein the processor further includes;

a first logic gate coupled to the storage unit, the logic gate generating a first signal in response to the control bit in the storage unit, the first logic gate generating a first signal when the processor is executing a interruptible code portion; and

a second logic gate coupled to the first logic gate, the second logic gate generating a halt signal in response to a halt request signal and the first signal.